

Parallel Programming and High-Performance Computing

Part 2: High-Performance Networks

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2 High-Performance Networks

Overview

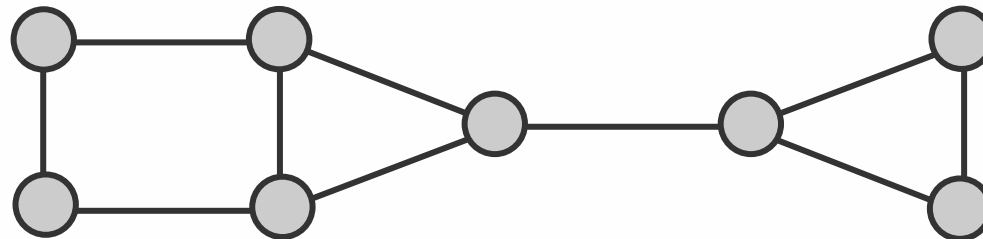
- some definitions
- (more) practical definitions
- static network topologies
- dynamic network topologies
- examples

*640k is enough for anyone,
and by the way, what's a network?*
—William Gates III,
chairman Microsoft Corp., 1984

2 High-Performance Networks

Some Definitions

- basic principles: graph theory
 - networks to be considered as bidirectional graphs with
 - nodes, i. e. processing elements
 - edges, i. e. connections between processing elements

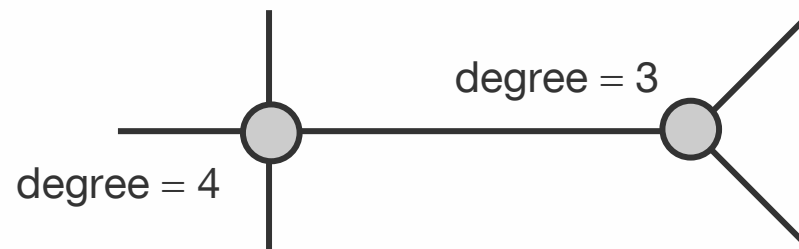


- *important questions*: communication time, amount of messages to be transmitted in parallel, fault tolerance, costs, ...

2 High-Performance Networks

Some Definitions

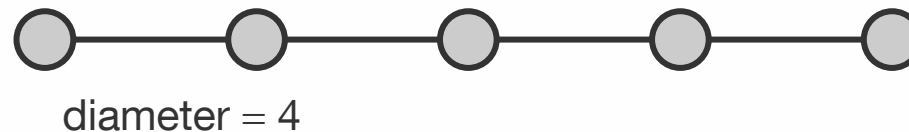
- **degree (node degree)**
 - number of connections (incoming and outgoing) between this node and other nodes
 - degree of a network = max. degree of all nodes in the network
 - higher degrees lead to
 - more parallelism and bandwidth for the communication
 - more costs (due to a higher amount of connections)
- objective: keep degree and, thus, costs small



2 High-Performance Networks

Some Definitions

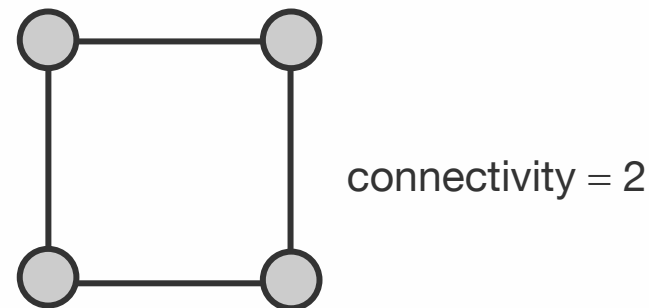
- diameter
 - distance of a pair of nodes (length of the shortest path between a pair of nodes), i. e. the amount of nodes a message has to pass on its way from the sender to the receiver
 - diameter of a network = max. distance of all pair of nodes in the network
 - higher diameters (between two nodes) lead to
 - longer communications
 - less fault tolerance (due to the higher amount of nodes that have to work properly)
- objective: small diameter



2 High-Performance Networks

Some Definitions

- **connectivity**
 - min. amount of edges (cables) that have to be removed to disconnect the network, i. e. the network falls apart into two loose sub-networks
 - higher connectivity leads to
 - more independent paths between two nodes
 - better fault tolerance (due to more routing possibilities)
 - faster communication (due to the avoidance of congestions in the network)
 - objective: high connectivity



2 High-Performance Networks

Some Definitions

- **complexity / costs**
 - amount of necessary hardware for the realisation of the network (network cards, cables, switches, e. g.)
 - higher complexity / costs due to more hardware

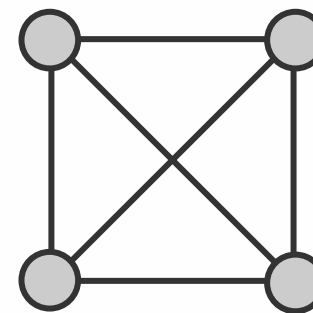
- **regularity**
 - extent of deviation in local network quantities (degree, connectivity, e. g.)
 - more regular quantities are easier to implement

- **length of lines**
 - physical length of the connections
 - shorter lengths of lines (for all connections) are advantageous

2 High-Performance Networks

Some Definitions

- **bisection width**
 - min. amount of edges (cables) that have to be removed to separate the network into two equal parts (bisection width \neq connectivity, see below)
 - important for determining the amount of messages that can be transmitted in parallel between one half of the nodes to the other half without the repeated usage of any connection
 - extreme case: Ethernet with bisection width = 1
 - objective: high bisection width (ideal: amount of nodes/2)



bisection width = 4
(connectivity = 3)

2 High-Performance Networks

Some Definitions

- **blocking**
 - a desired connection between two nodes cannot be established due to already existing connections between other pairs of nodes
 - objective: non-blocking networks

- **extensibility**
 - in which steps the network can be extended (arbitrarily or only by doubling the amount of nodes, e. g.)

- **scalability**
 - keeping the essential properties of the network under any increase of the amount of nodes

2 High-Performance Networks

Some Definitions

- **fault tolerance (redundancy)**
 - connections between (arbitrary) nodes can still be established even under the breakdown of single components
 - a fault-tolerant network has to provide at least one redundant path between all arbitrary pairs of nodes
 - *graceful degradation*: the ability of a system to stay functional (maybe with less performance) even under the breakdown of single components

- **complexity of routing**
 - costs for determining a route for a message from the sender to the receiver
 - objective: routing should be simple (to be implemented in hardware)

2 High-Performance Networks

Overview

- some definitions
- (more) practical definitions
- static network topologies
- dynamic network topologies
- examples

2 High-Performance Networks

Practical Definitions

- **bandwidth**
 - max. transmission performance of a network for a certain amount of time
 - bandwidth B in general measured as megabits or megabytes per second (Mbps or MBps, resp.), nowadays more often as gigabits or gigabytes per second (Gbps or GBps, resp.)

- **bisection bandwidth**
 - max. transmission performance of a network over the bisection line, i. e. sum of single bandwidths from all edges (cables) that are “cut” when bisecting the network
 - thus bisection bandwidth is a *measure of bottleneck bandwidth*
 - units are same as for bandwidth

2 High-Performance Networks

Practical Definitions

- **latency**
 - delay time of a communication (time between sending and receiving the head of a message)
 - latency L measured in seconds
- **transmission time (delay)**
 - time for transmitting an entire message between two nodes
 - transmission time depends on the size S of a message
 - in case there are no conflicts, the transmission time can be computed as follows

$$d(S) = L + S/B$$

- sometimes this is also referred to as *delay*

2 High-Performance Networks

Practical Definitions

- throughput
 - ideal case: bandwidth = throughput (S_{max})
 - mostly, the (theoretical) bandwidth is not achieved with common message sizes
 - throughput to be computed as ratio between message size and delay

$$p(S) = S / d(S)$$

- throughput interesting for determination of *half-power-point*: message size S_H at which half of the bandwidth B is being achieved
- example: $L = 10\mu s$, $B = 10MBps$

$$\frac{1}{2}B = S_H / d(S_H) = S_H / (L + S_H/B) \Rightarrow S_H = B \cdot L \Rightarrow S_H = 0.1kB$$

2 High-Performance Networks

Overview

- some definitions
- (more) practical definitions
- **static network topologies**
- dynamic network topologies
- examples

2 High-Performance Networks

Static Network Topologies

- to be distinguished
 - *static networks*
 - fixed connections between pairs of nodes
 - control functions are done by the nodes or by special connection hardware
 - *dynamic networks*
 - no fixed connections between pairs of nodes
 - all nodes are connected via inputs and outputs to a so called switching component
 - control functions are concentrated in the switching component
 - various routes can be switched

2 High-Performance Networks

Static Network Topologies

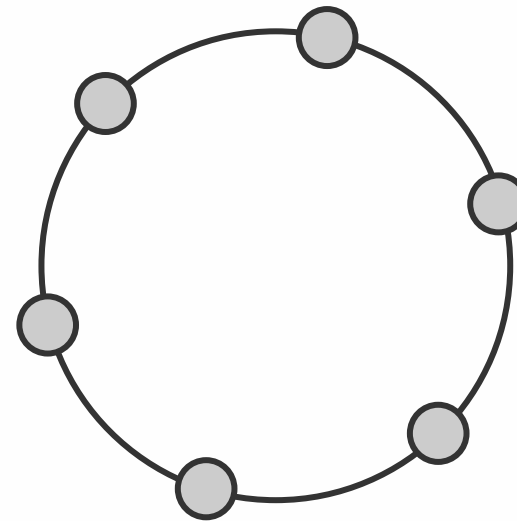
- chain (linear array)
 - one-dimensional network
 - N nodes and $N-1$ edges
 - degree = 2
 - diameter = $N-1$
 - bisection width = 1
 - drawback: too slow for large N



2 High-Performance Networks

Static Network Topologies

- ring
 - two-dimensional network
 - N nodes and N edges
 - degree = 2
 - diameter = $\lfloor N/2 \rfloor$
 - bisection width = 2
 - drawback: too slow for large N
 - how about fault tolerance?

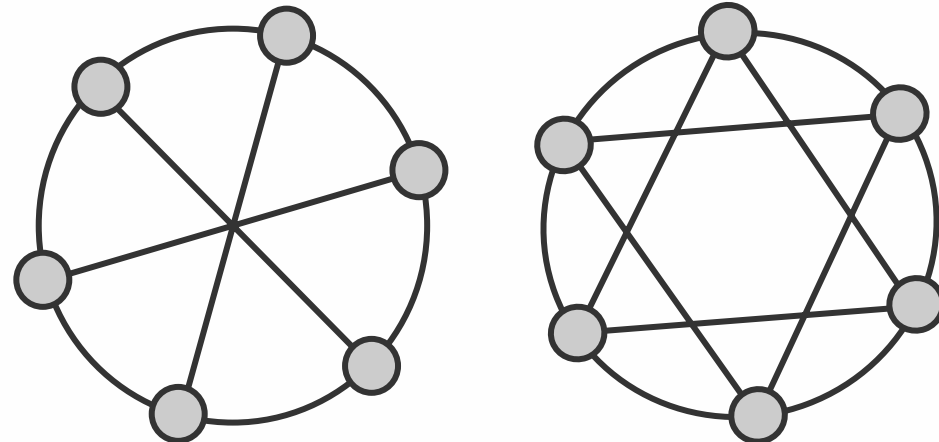


2 High-Performance Networks

Static Network Topologies

- chordal ring
 - two-dimensional network
 - N nodes and $3N/2, 4N/2, 5N/2, \dots$ edges
 - degree = 3, 4, 5, ...
 - higher degrees lead to
 - smaller diameters
 - higher fault tolerance (due to redundant connections)
 - drawback: higher costs

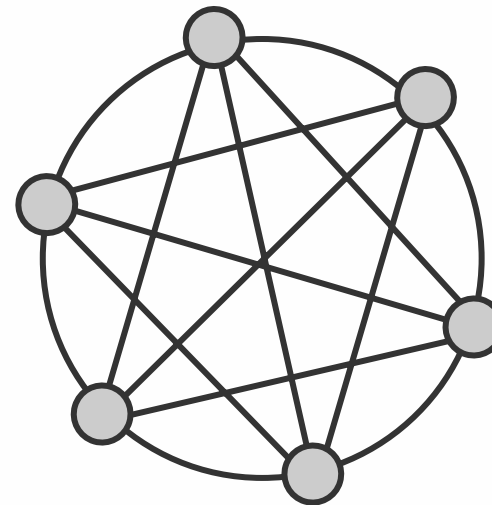
ring with degree = 3 (left)
and degree = 4 (right)



2 High-Performance Networks

Static Network Topologies

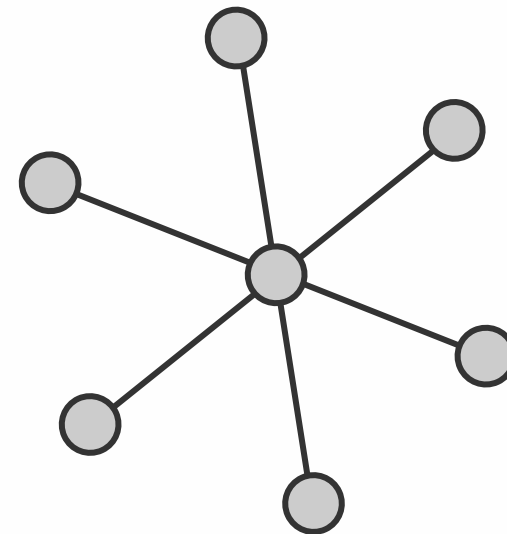
- **completely connected**
 - two-dimensional network
 - N nodes and $N \cdot (N-1) / 2$ edges
 - degree = $N-1$
 - diameter = 1
 - bisection width = $\lfloor N/2 \rfloor \cdot \lceil N/2 \rceil$
 - very high fault tolerance
 - drawback: too expensive for large N



2 High-Performance Networks

Static Network Topologies

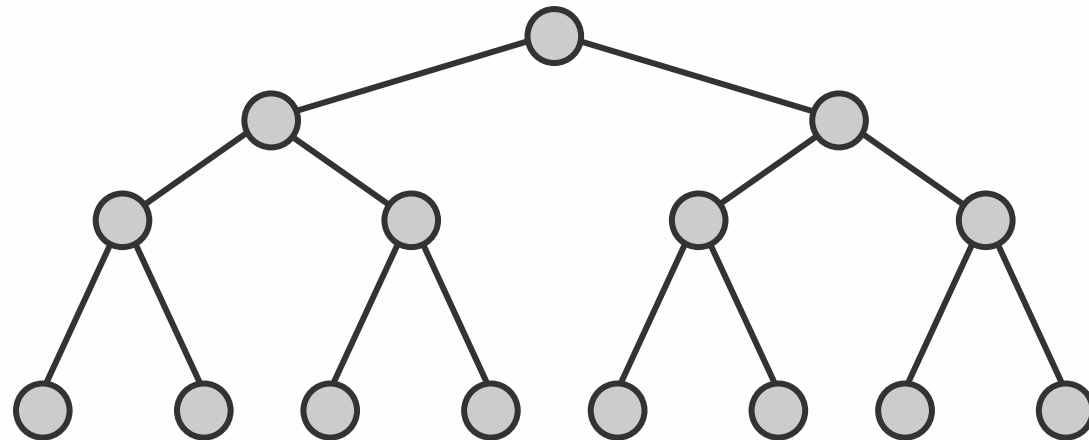
- star
 - two-dimensional network
 - N nodes and $N-1$ edges
 - degree = $N-1$
 - diameter = 2
 - bisection width = $\lfloor N/2 \rfloor$
 - drawback: bottleneck in central node



2 High-Performance Networks

Static Network Topologies

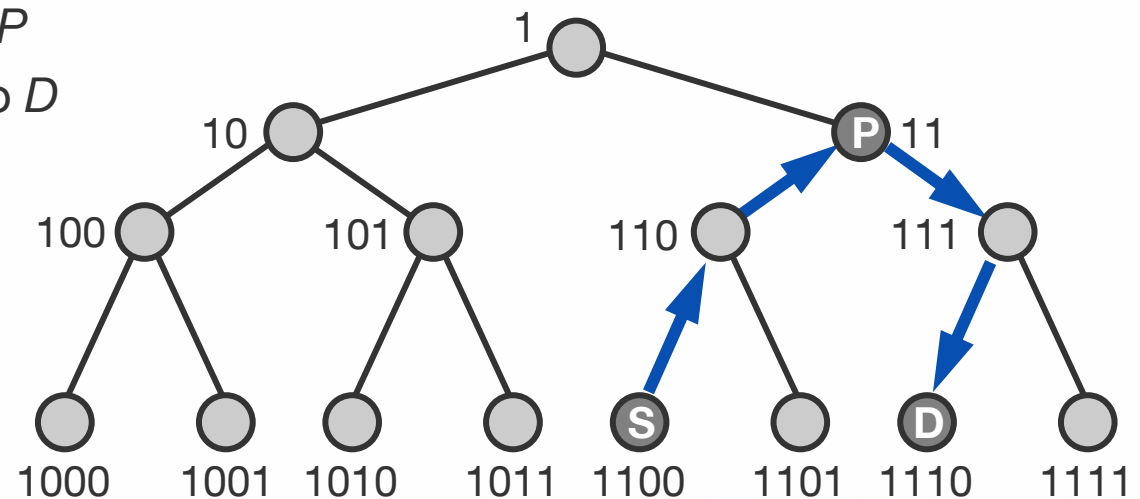
- **binary tree**
 - two-dimensional network
 - N nodes and $N-1$ edges (tree height $h = \lfloor \log N \rfloor$)
 - degree = 3
 - diameter = $2h$
 - bisection width = 1
 - drawback: bottleneck in direction of root (→ blocking)



2 High-Performance Networks

Static Network Topologies

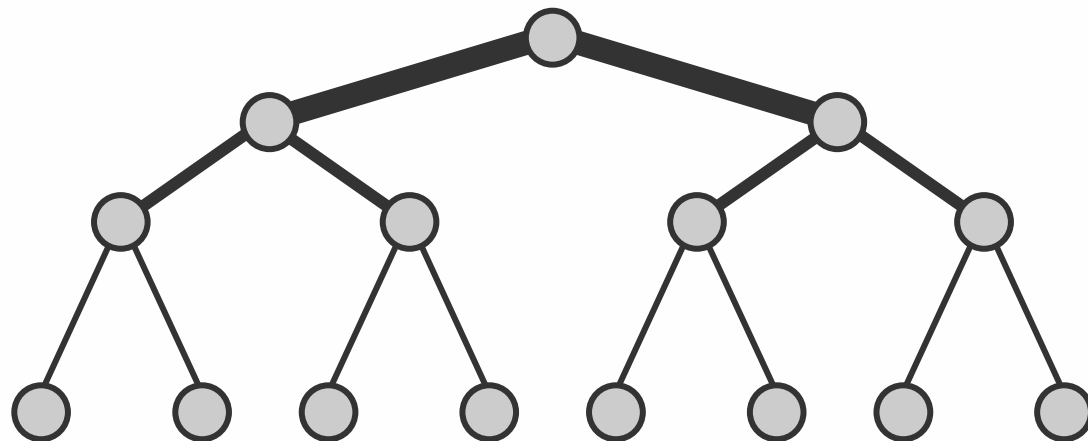
- binary tree (cont'd)
 - addressing
 - label on level m consists of m bits; root has label “1”
 - suffix “0” is added to left son, suffix “1” is added to right son
 - routing
 - find common parent node P of nodes S and D
 - ascend from S to P
 - descend from P to D



2 High-Performance Networks

Static Network Topologies

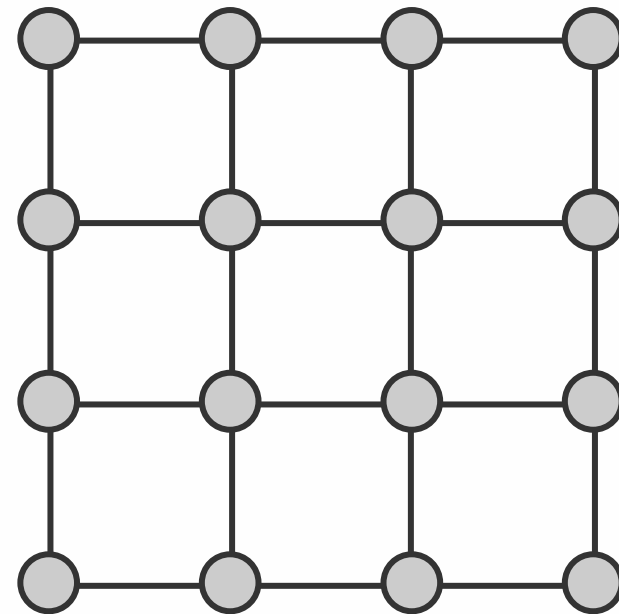
- binary tree (cont'd)
 - solution to overcome the bottleneck → fat tree
 - edges on level m get higher priority than edges on level $m+1$
 - capacity is doubled on each higher level
 - now, bisection width = 2^{h-2}
 - frequently used: HLRB II, e. g.



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Static Network Topologies

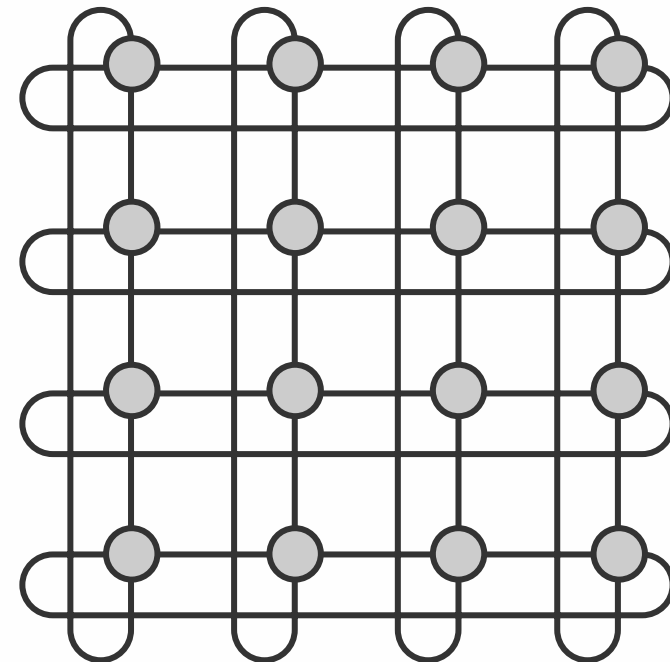
- mesh / torus
 - k -dimensional network
 - N nodes and $k \cdot (N-r)$ edges ($r \times r$ mesh, $r = \sqrt[k]{N}$)
 - degree = $2k$
 - diameter = $k \cdot (r-1)$
 - bisection width = r^{k-1}
 - high fault tolerance
 - drawback
 - large diameter
 - too expensive for $k > 3$



2 High-Performance Networks

Static Network Topologies

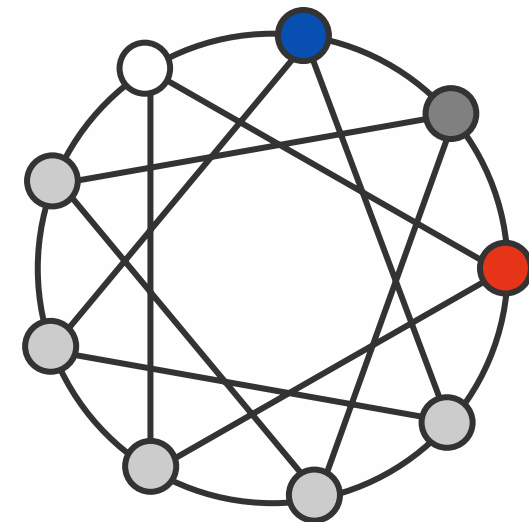
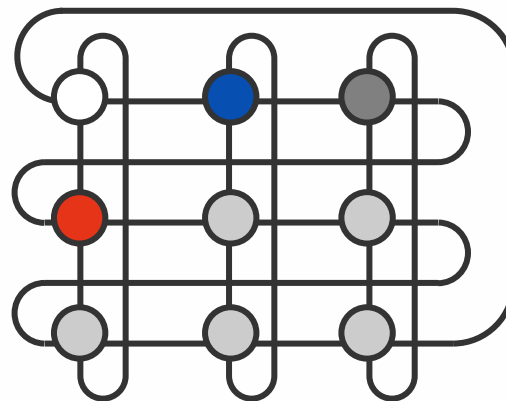
- mesh / torus (cont'd)
 - k -dimensional mesh with cyclic connections in each dimension
 - N nodes and $k \cdot N$ edges ($r \times r$ mesh, $r = \sqrt[k]{N}$)
 - diameter = $k \cdot \lfloor r/2 \rfloor$
 - bisection width = $2r^{k-1}$
 - frequently used: BlueGene/L, e. g.
 - drawback: too expensive for $k > 3$



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Static Network Topologies

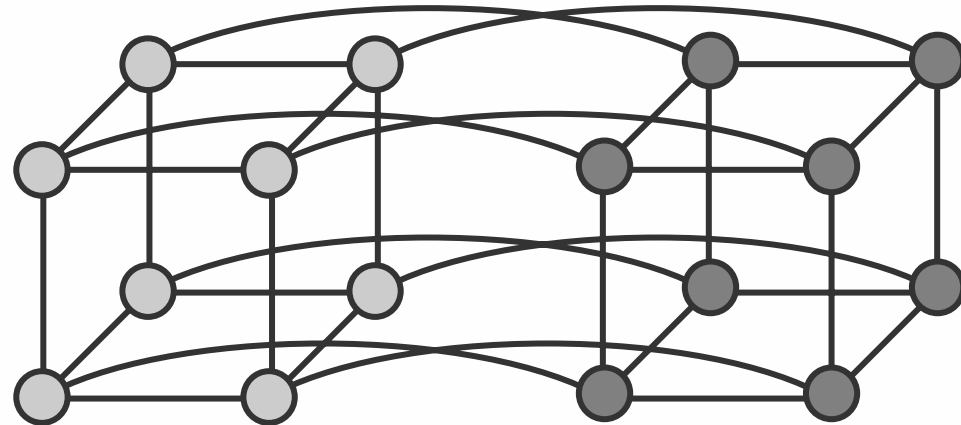
- ILLIAC mesh
 - two-dimensional network
 - N nodes and $2N$ edges ($r \times r$ mesh, $r = \sqrt{N}$)
 - degree = 4
 - diameter = $r-1$
 - bisection width = $2r$
 - conforms to a chordal ring of degree = 4



2 High-Performance Networks

Static Network Topologies

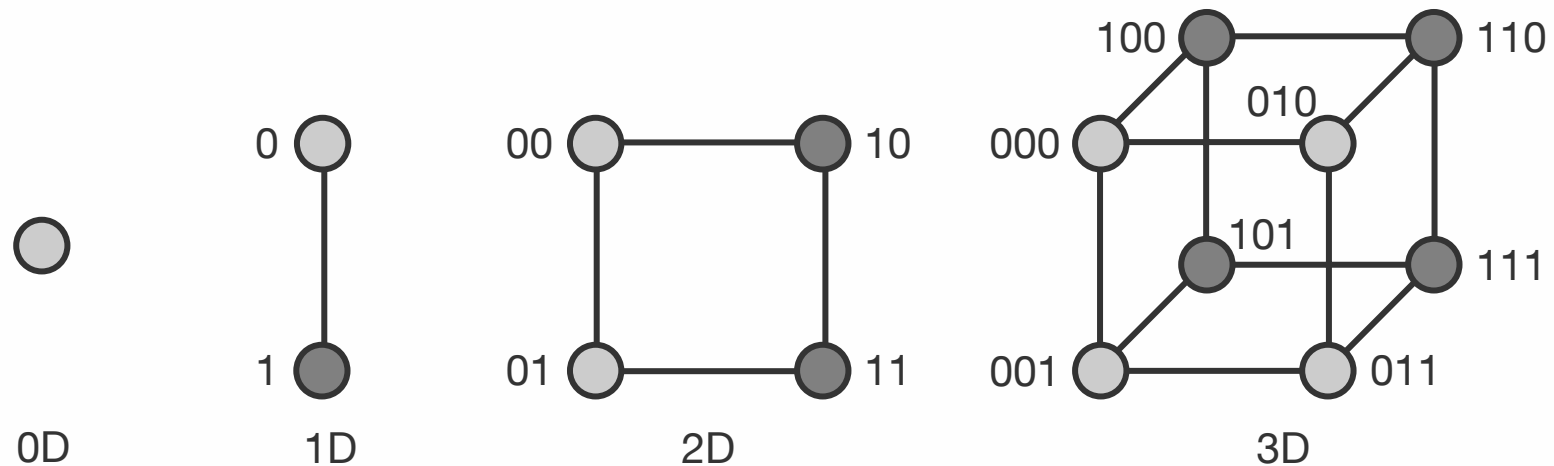
- hypercube
 - k -dimensional network
 - 2^k nodes and $k \cdot 2^{k-1}$ edges
 - degree = k
 - diameter = k
 - bisection width = 2^{k-1}
 - drawback: scalability (only doubling of nodes allowed)



2 High-Performance Networks

Static Network Topologies

- hypercube (cont'd)
 - principle design
 - construction of a k -dimensional hypercube via connection of the corresponding nodes of two $k-1$ -dimensional hypercubes
 - inherent labelling via adding prefix “0” to one sub-cube and prefix “1” to the other sub-cube



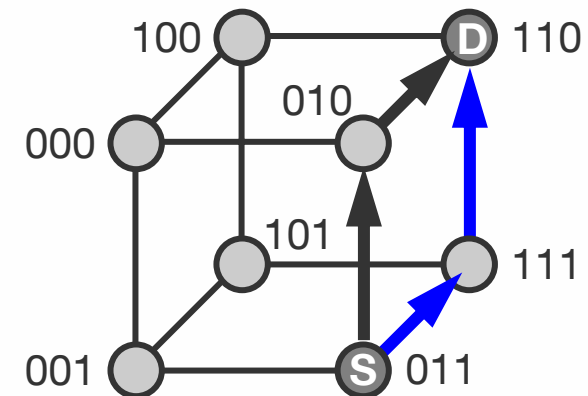
2 High-Performance Networks

Static Network Topologies

- hypercube (cont'd)
 - nodes are directly connected for a HAMMING distance of 1 only
 - routing
 - compute $S \otimes D$ (xor) for possible ways between nodes S and D
 - route frames in increasingly / decreasingly order until final destination is reached

- example

- $S = "011", D = "110"$
- $S \otimes D = "101"$
- decreasing: $"011" \Rightarrow "010" \Rightarrow "110"$
- increasing: $"011" \Rightarrow "111" \Rightarrow "110"$



2 High-Performance Networks

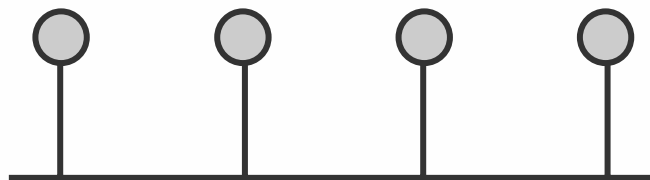
Overview

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- (more) practical definitions
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- dynamic network topologies
- examples

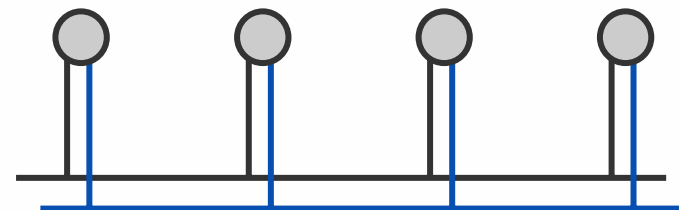
2 High-Performance Networks

Dynamic Network Topologies

- bus
 - simple and cheap single stage network
 - shared usage from all connected nodes, thus, just one frame transfer at any point in time
 - frame transfer in one step (i. e. diameter = 1)
 - good extensibility, but bad scalability
 - fault tolerance only for multiple bus systems
 - example: Ethernet



single bus

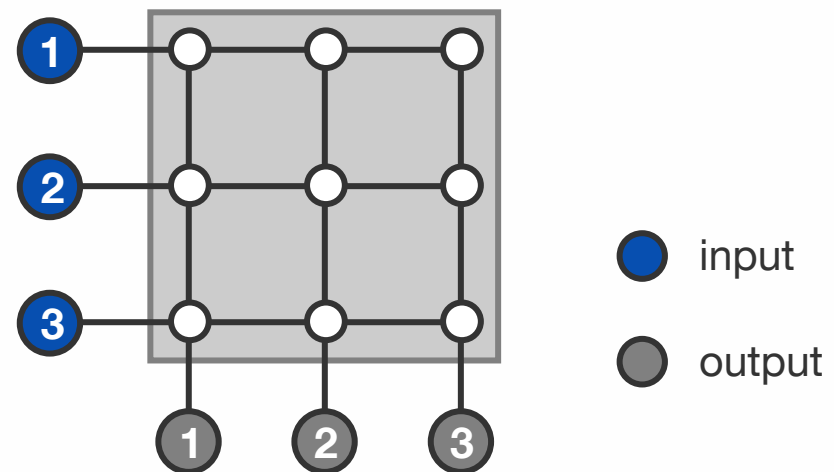
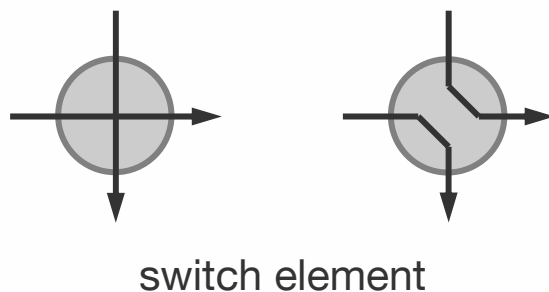


multiple bus (here dual)

2 High-Performance Networks

Dynamic Network Topologies

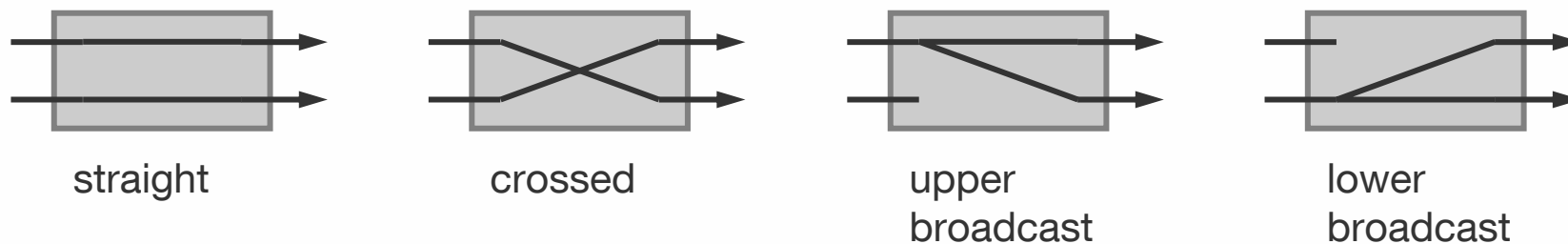
- crossbar
 - completely connected network with all possible permutations of N inputs and N outputs (in general $N \times M$ inputs / outputs)
 - switch elements allow simultaneous communication between all possible disjoint pairs of inputs and outputs without blocking
 - very fast (diameter = 1), but expensive due to N^2 switch elements
 - used for processor—processor and processor—memory coupling
 - example: The Earth Simulator



2 High-Performance Networks

Dynamic Network Topologies

- permutation networks
 - tradeoff between low performance of buses and high hardware costs of crossbars
 - often 2×2 crossbar as basic element
 - N inputs can simultaneously be switched to N outputs → permutation of inputs (to outputs)
 - single stage: consists of one column of 2×2 switch elements
 - multistage: consists of several of those columns



2 High-Performance Networks

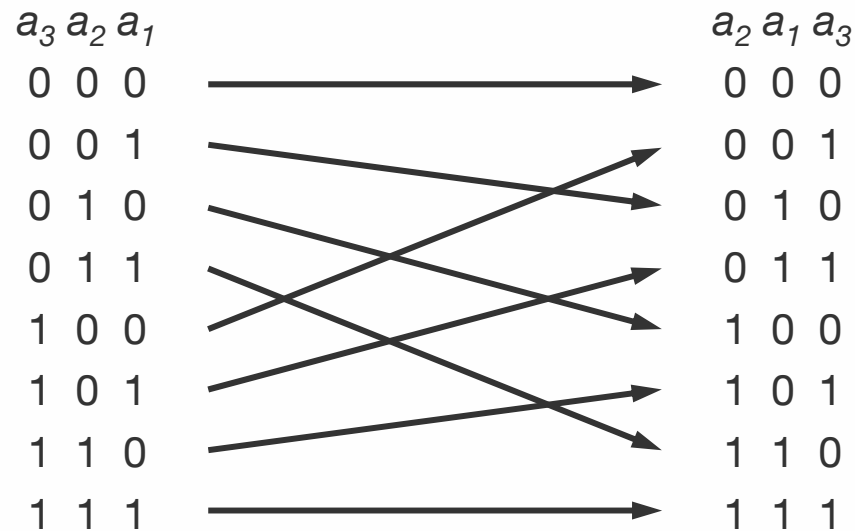
Dynamic Network Topologies

- permutation networks (cont'd)
 - permutations: unique (bijective) mapping of inputs to outputs
 - addressing
 - label inputs from 0 to $2N-1$ (in case of N switch elements)
 - write labels in binary representation $(a_K, a_{K-1}, \dots, a_2, a_1)$
 - permutations can now be expressed as simple bit manipulation
 - typical permutations
 - perfect shuffle
 - butterfly
 - exchange

2 High-Performance Networks

Dynamic Network Topologies

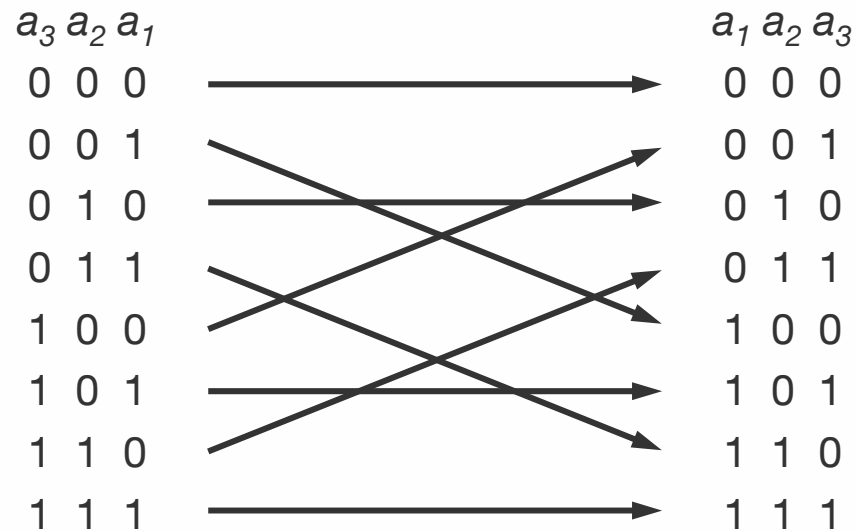
- permutation networks (cont'd)
 - perfect shuffle permutation
 - cyclic left shift
 - $P(a_K, a_{K-1}, \dots, a_2, a_1) \rightarrow (a_{K-1}, \dots, a_2, a_1, a_K)$



2 High-Performance Networks

Dynamic Network Topologies

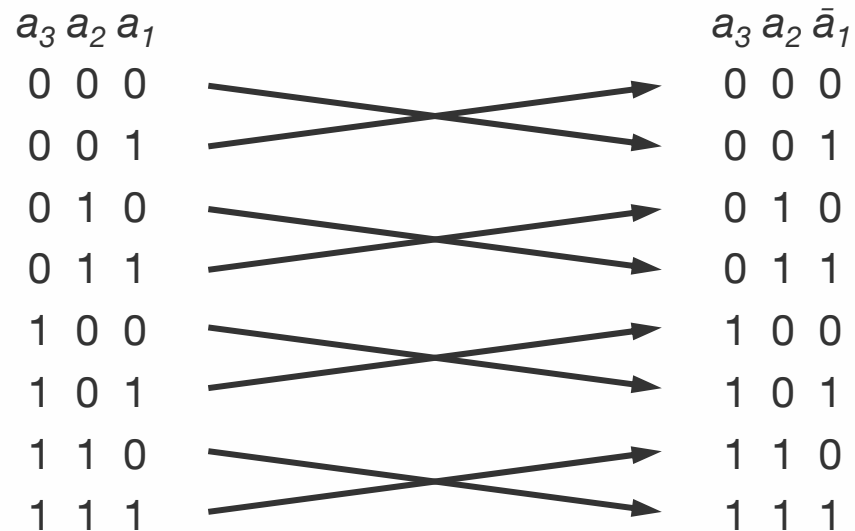
- permutation networks (cont'd)
 - butterfly permutation
 - exchange of first / highest and last / lowest bit
 - $B(a_K, a_{K-1}, \dots, a_2, a_1) \rightarrow (a_1, a_{K-1}, \dots, a_2, a_K)$



2 High-Performance Networks

Dynamic Network Topologies

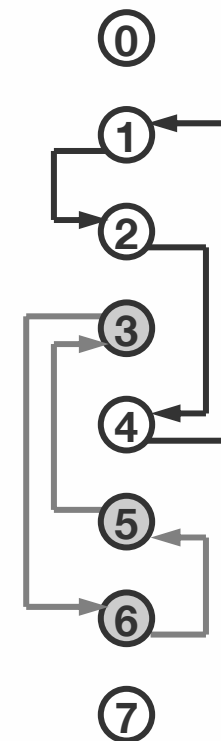
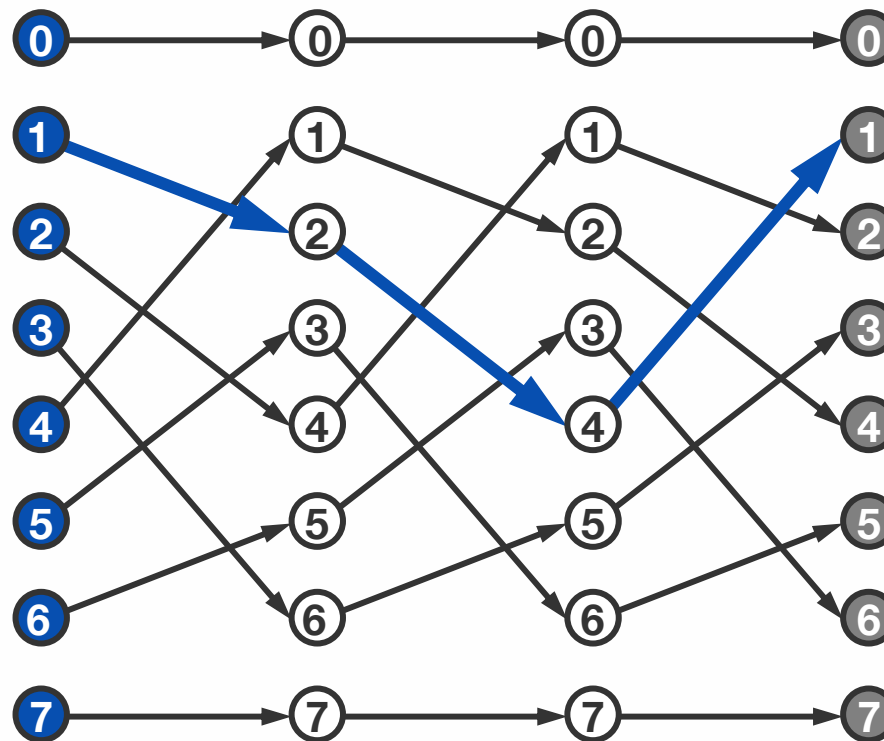
- permutation networks (cont'd)
 - exchange permutation
 - negation of last / lowest bit
 - $E(a_K, a_{K-1}, \dots, a_2, a_1) \rightarrow (a_K, a_{K-1}, \dots, a_2, \bar{a}_1)$



2 High-Performance Networks

Dynamic Network Topologies

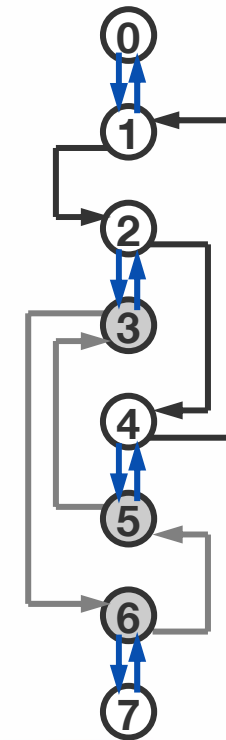
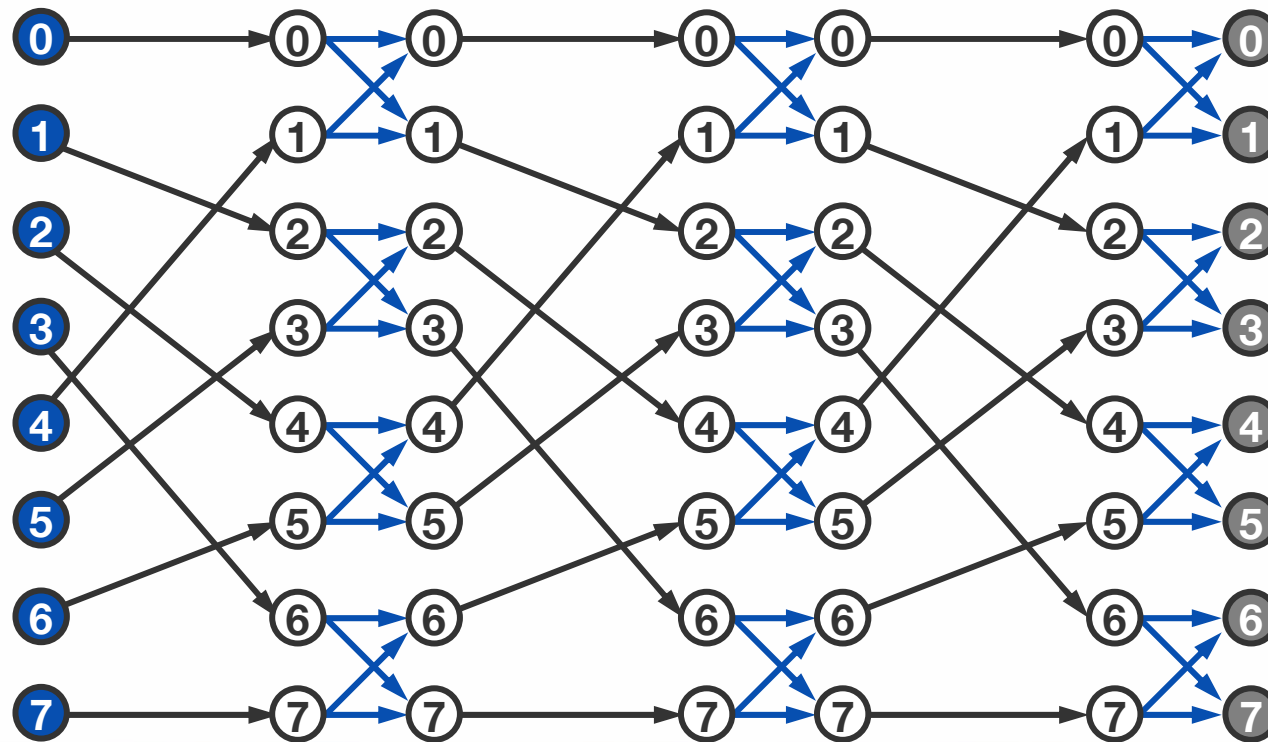
- permutation networks (cont'd)
 - example: perfect shuffle connection pattern
 - problem: not all destinations are accessible from a source



2 High-Performance Networks

Dynamic Network Topologies

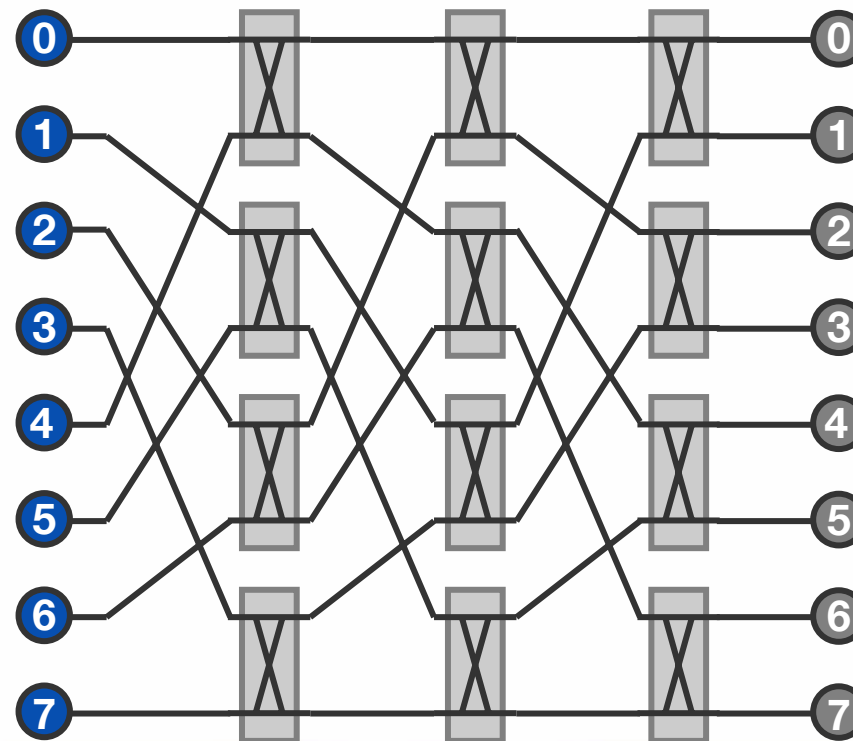
- permutation networks (cont'd)
 - adding additional exchange permutations (→ shuffle-exchange)
 - all destinations are now accessible from any source



2 High-Performance Networks

Dynamic Network Topologies

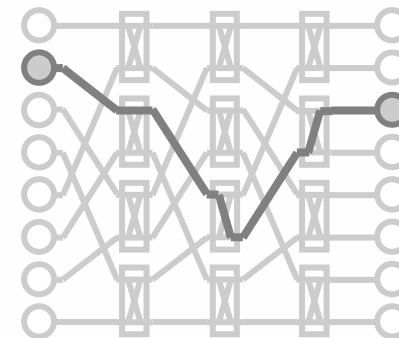
- **omega**
 - based on the shuffle-exchange connection pattern
 - exchange permutations replaced by 2×2 switch elements



2 High-Performance Networks

Dynamic Network Topologies

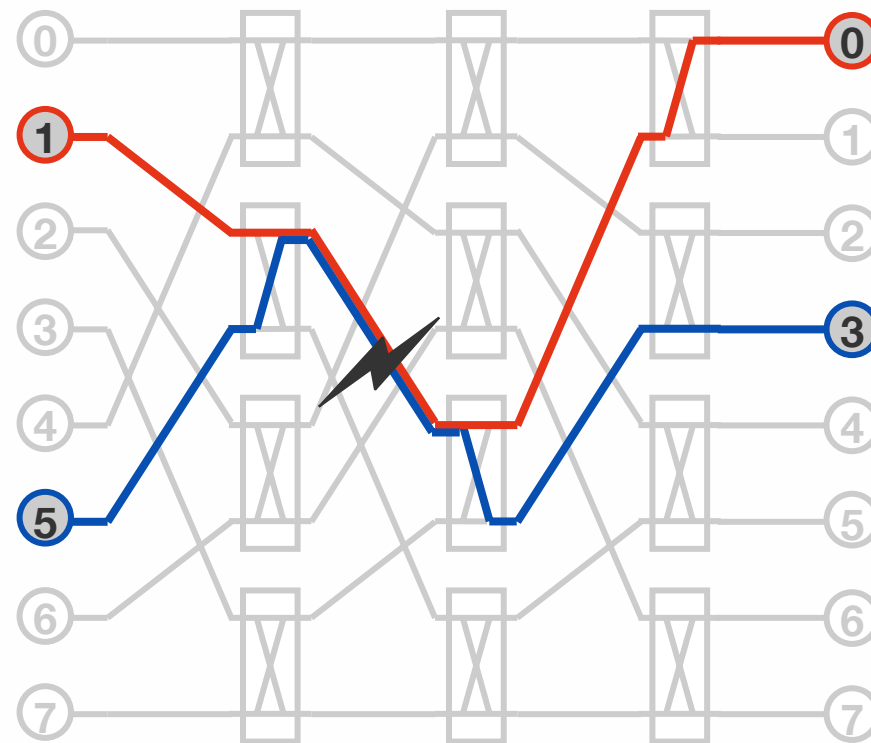
- **omega (cont'd)**
 - multistage network
 - N nodes and $E = N/2 \cdot (\log N)$ switch elements
 - diameter = $\log N$ (all stages have to be passed)
 - $N!$ permutations possible, but only 2^E different switch states
 - (self configuring) routing
 - compare addresses from S and D bitwise from left to right, i. e. stage i evaluates address bits s_i and d_i
 - if equal switch straight (–), otherwise switch crossed (×)
- example
 - $S = "001"$, $D = "010"$
 - switch states: – × ×



2 High-Performance Networks

Dynamic Network Topologies

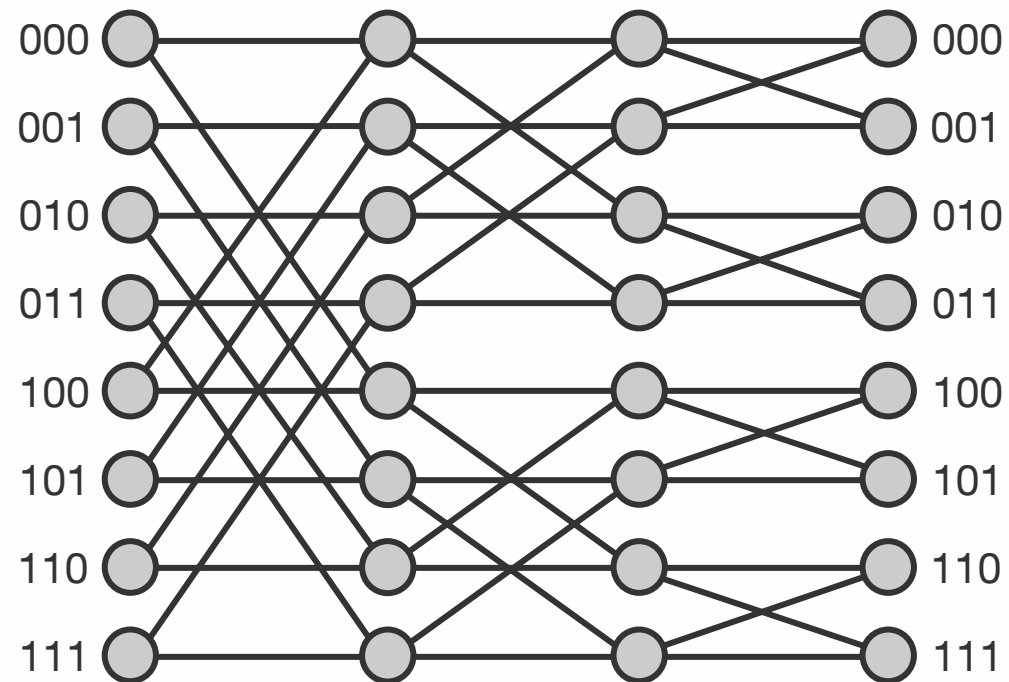
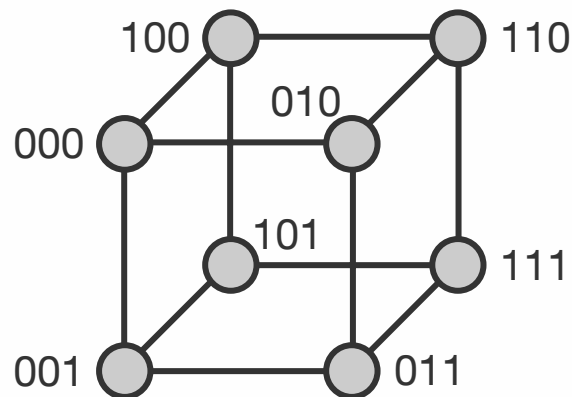
- omega (cont'd)
 - omega is a *bidelta network* → operates also backwards
 - drawback: blocking possible



2 High-Performance Networks

Dynamic Network Topologies

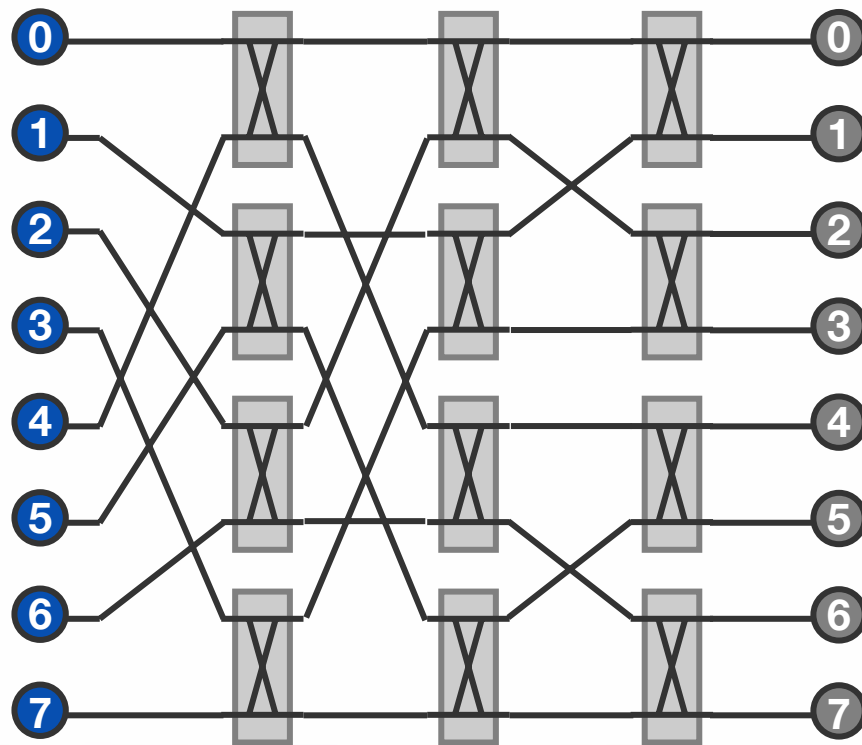
- banyan / butterfly
 - idea: unrolling of a static hypercube
 - bitwise processing of address bits a_i from left to right → dynamic hypercube a. k. a. butterfly (known from FFT flow diagram)



2 High-Performance Networks

Dynamic Network Topologies

- banyan / butterfly (cont'd)
 - replace crossed connections by 2×2 switch elements
 - introduced by GOKE and LIPOVSKI in 1973; blocking still possible

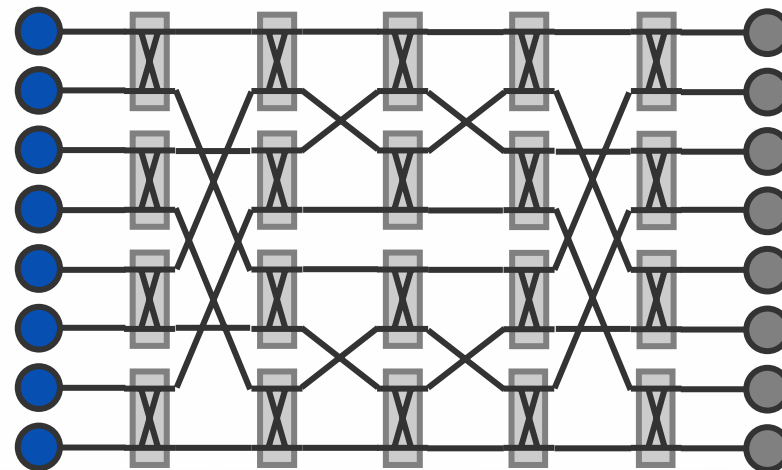


banyan tree

2 High-Performance Networks

Dynamic Network Topologies

- **BENEŠ**
 - multistage network
 - butterfly merged at the last column with its copied mirror
 - N nodes and $N \cdot (\lg N) - N/2$ switch elements
 - diameter = $2(\lg N) - 1$
 - $N!$ permutations possible, all can be switched
 - key property: for any permutation of inputs to outputs there is a contention-free routing



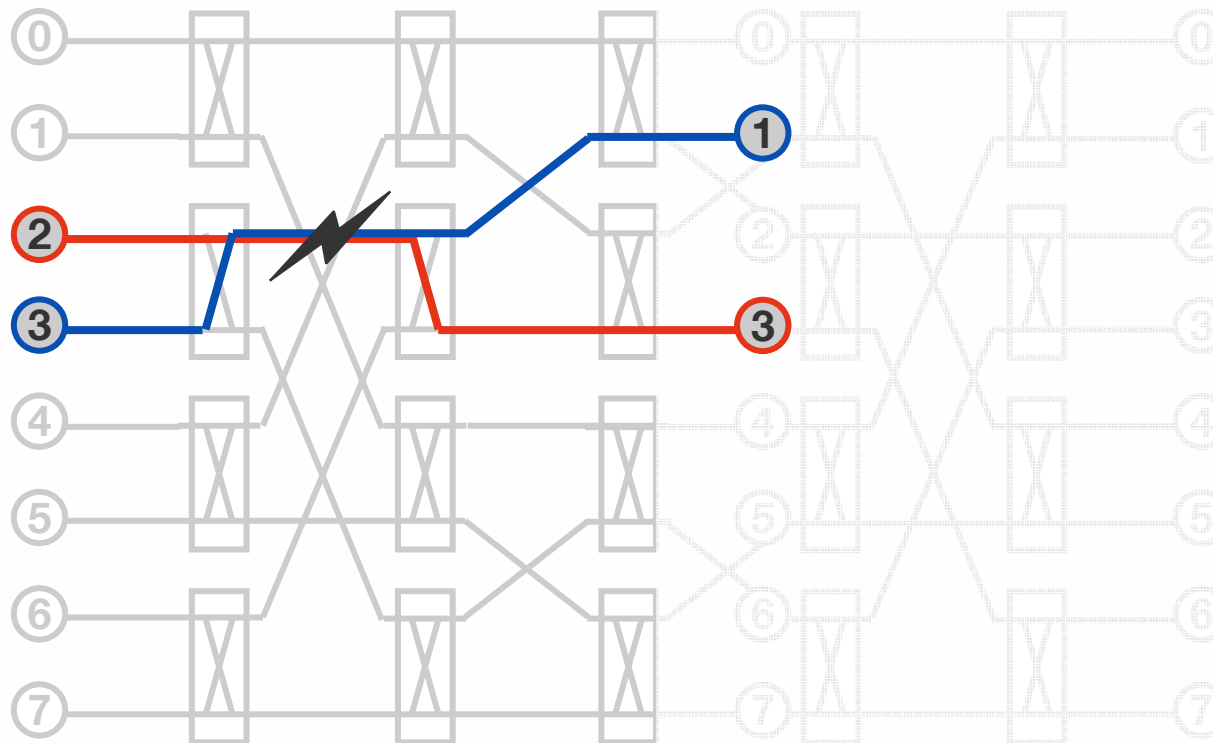
2 High-Performance Networks

Dynamic Network Topologies

- BENEŠ (cont'd)

- example

- $S_1 = 2, D_1 = 3$ and $S_2 = 3, D_2 = 1$ → blocking for butterfly



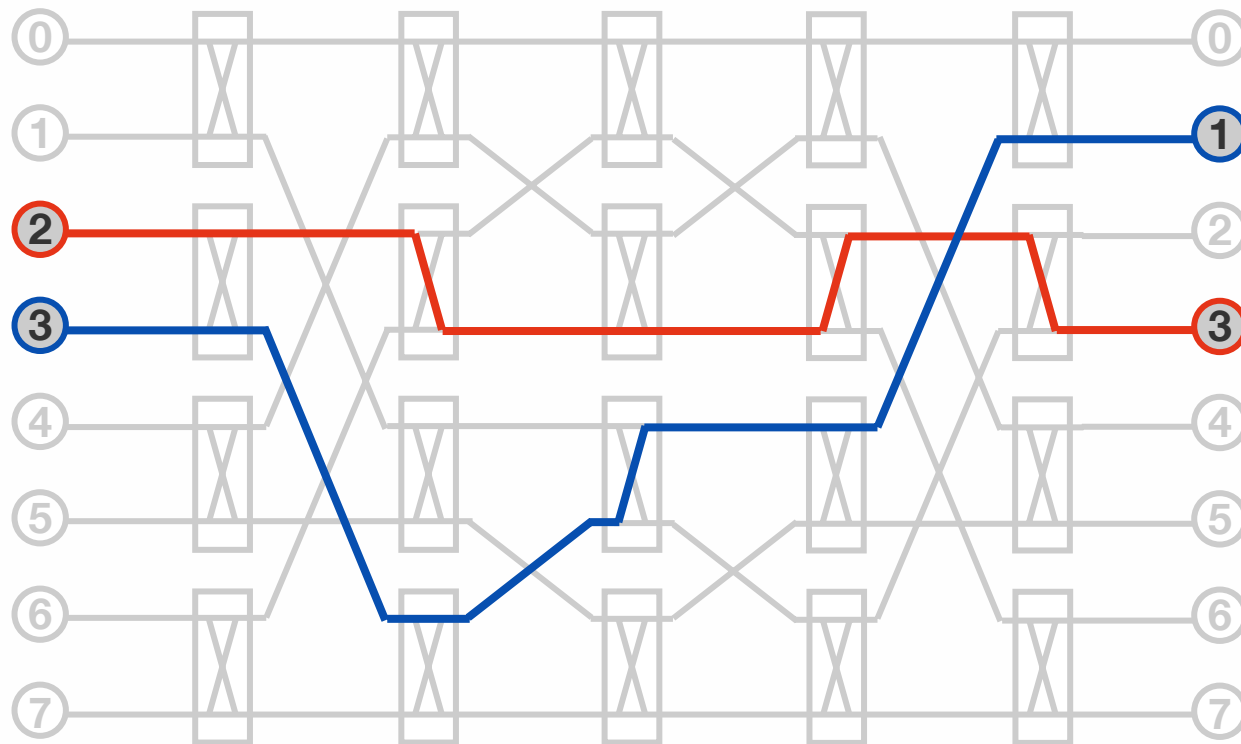
2 High-Performance Networks

Dynamic Network Topologies

- BENEŠ (cont'd)

- example

- $S_1 = 2, D_1 = 3$ and $S_2 = 3, D_2 = 1 \rightarrow$ no blocking for BENEŠ



2 High-Performance Networks

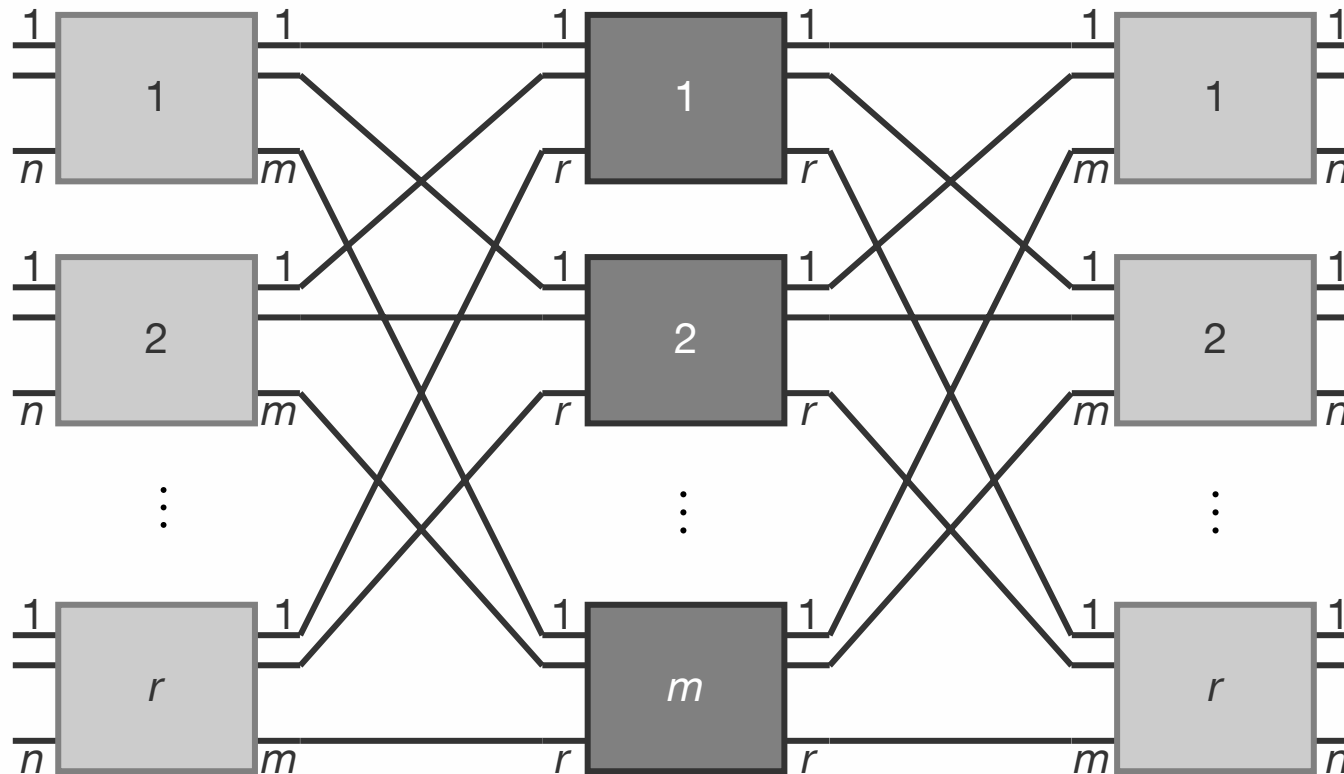
Dynamic Network Topologies

- CLOS
 - proposed by CLOS in 1953 for telephone switching systems
 - objective: to overcome the costs of crossbars (N^2 switch elements)
 - idea
 - replace the entire crossbar with three stages of smaller ones
 - *ingress stage*: R crossbars with $N \times M$ inputs / outputs
 - *middle stage*: M crossbars with $R \times R$ inputs / outputs
 - *egress stage*: R crossbars with $M \times N$ inputs / outputs
 - thus much fewer switch elements than for the entire system
 - any incoming frame is routed from the input via one of the middle stage crossbars to the respective output
 - a middle stage crossbar is available if both links to the ingress and egress stage are free

2 High-Performance Networks

Dynamic Network Topologies

- CLOS (cont'd)
 - $R \cdot N$ inputs can be assigned to $R \cdot N$ outputs



2 High-Performance Networks

Dynamic Network Topologies

- CLOS (cont'd)
 - relative values of M and N define the blocking characteristics
 - $M \geq N$: *rearrangeable non-blocking*
 - a free input can always be connected to a free output
 - existing connections might be assigned to different middle stage crossbars (rearrangement)
 - $M \geq 2N-1$: *strict-sense non-blocking*
 - a free input can always be connected to a free output
 - no re-assignment necessary

2 High-Performance Networks

Dynamic Network Topologies

- CLOS (cont'd)
 - proof for $M \geq N$ via HALL's "Marriage Theorem" (1)

Let $G = (V_{IN}, V_{OUT}, E)$ be a bipartite graph. A *perfect matching* for G is an injective function $f : V_{IN} \rightarrow V_{OUT}$ so that for every $x \in V_{IN}$, there is an edge in E whose endpoints are x and $f(x)$. One would expect a perfect matching to exist if G contains "enough" edges, i. e. if for every subset $A \subset V_{IN}$ the image set $\delta A \subset V_{OUT}$ is sufficient large.

Theorem: G has a perfect matching if and only if for every subset $A \subset V_{IN}$ the inequality $|A| \leq |\delta A|$ holds.

Often explained as follows: Imagine two groups of N men and N women. If any subset of S boys (where $0 \leq S \leq N$) knows S or more girls, each boy can be married with a girl he knows.

2 High-Performance Networks

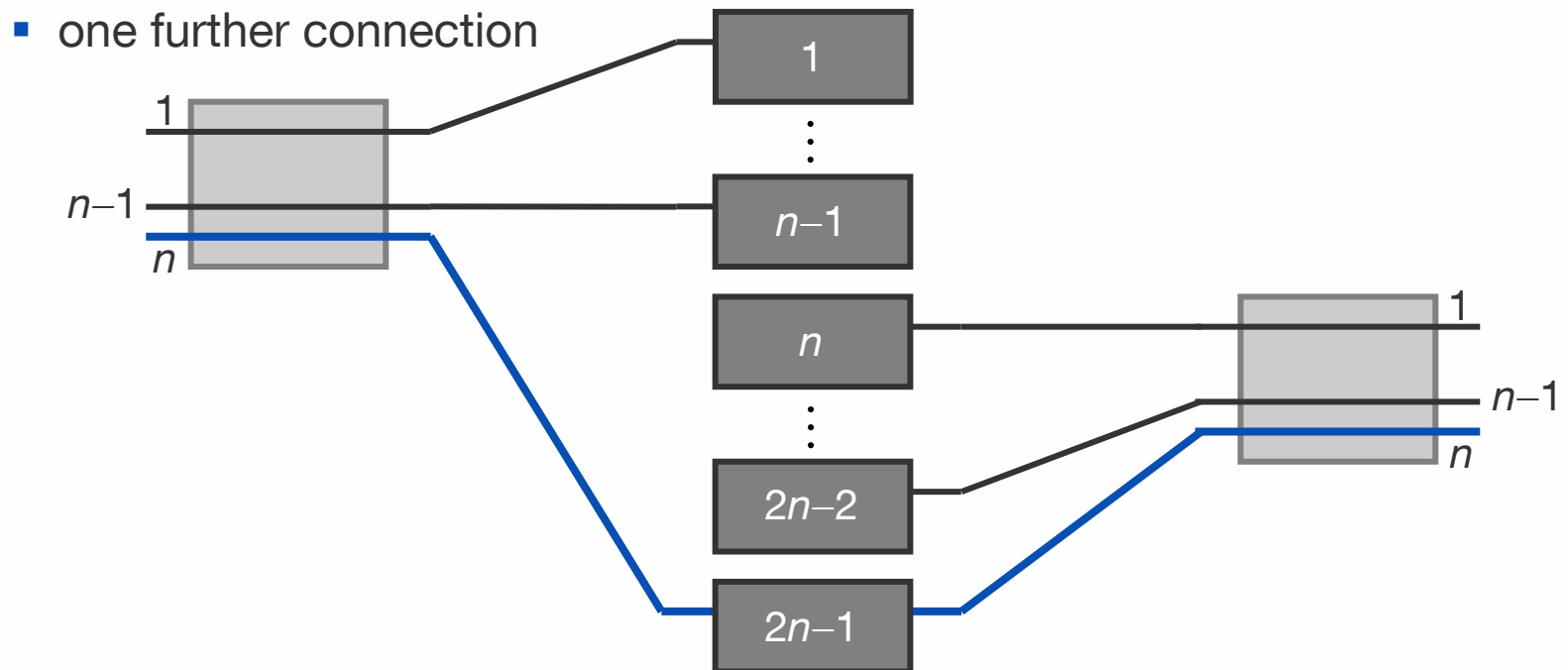
Dynamic Network Topologies

- CLOS (cont'd)
 - proof for $M \geq N$ via HALL's "Marriage Theorem" (2)
 - ▶ boy := ingress stage crossbar
 - ▶ girl := egress stage crossbar
 - ▶ a boy knows a girl if there exists a (direct) connection between them
 - ▶ assume there's one free input and one free output left
- 1) for $0 \leq S \leq R$ boys there are $S \cdot N$ connections \rightarrow at least S girls
 - 2) thus, HALL's theorem states there exists a perfect matching
 - 3) R connections can be handled by one middle stage crossbar
 - 4) bundle these connections and delete the middle stage crossbar
 - 5) repeat from step 1) until $M = 1$
 - 6) new connection can be handled, maybe rearrangement necessary \square

2 High-Performance Networks

Dynamic Network Topologies

- CLOS (cont'd)
 - proof for $M \geq 2N-1$ via worst case scenario
 - crossbar with $N-1$ inputs and crossbar with $N-1$ outputs, all connected to different middle stage crossbars



2 High-Performance Networks

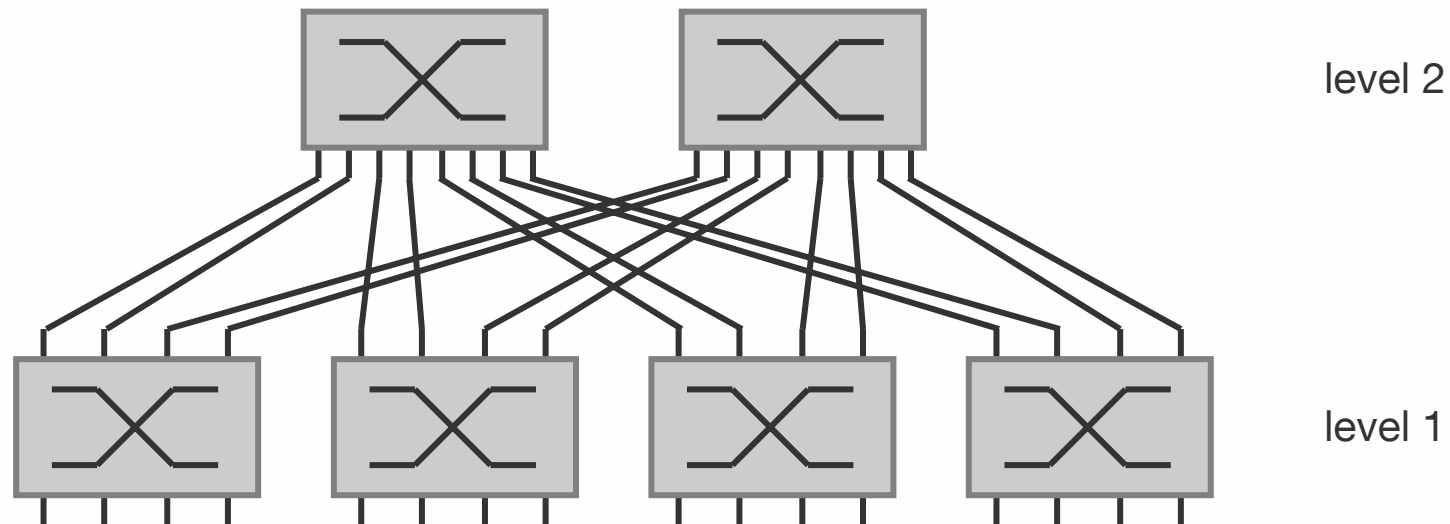
Dynamic Network Topologies

- constant bisection bandwidth
 - more general concept of CLOS and fat tree networks
 - construction of a non-blocking network connecting M nodes
 - using multiple levels of basic $N \times N$ switch elements ($M > N$)
 - for any given level, the downstream bandwidth (in direction to the nodes) is identical to the upstream bandwidth (in direction to the interconnection)
 - key for non-blocking: always preserve identical bandwidth (upstream and downstream) between any two levels
 - observation: for two-stage constant bisection bandwidth (CBB) networks connecting M nodes always $3M$ ports (i. e. sum of inputs and outputs) are necessary (each node needs two ports in the first and one port in the second stage)
 - frequently used: InfiniBand, e. g.

2 High-Performance Networks

Dynamic Network Topologies

- constant bisection bandwidth (cont'd)
 - example: CBB connecting 16 nodes with 4×4 switch elements
 - hence in total 48 ports (i. e. 6 switch elements) are necessary



2 High-Performance Networks

Overview

- some definitions
- (more) practical definitions
- static network topologies
- dynamic network topologies
- examples

2 High-Performance Networks

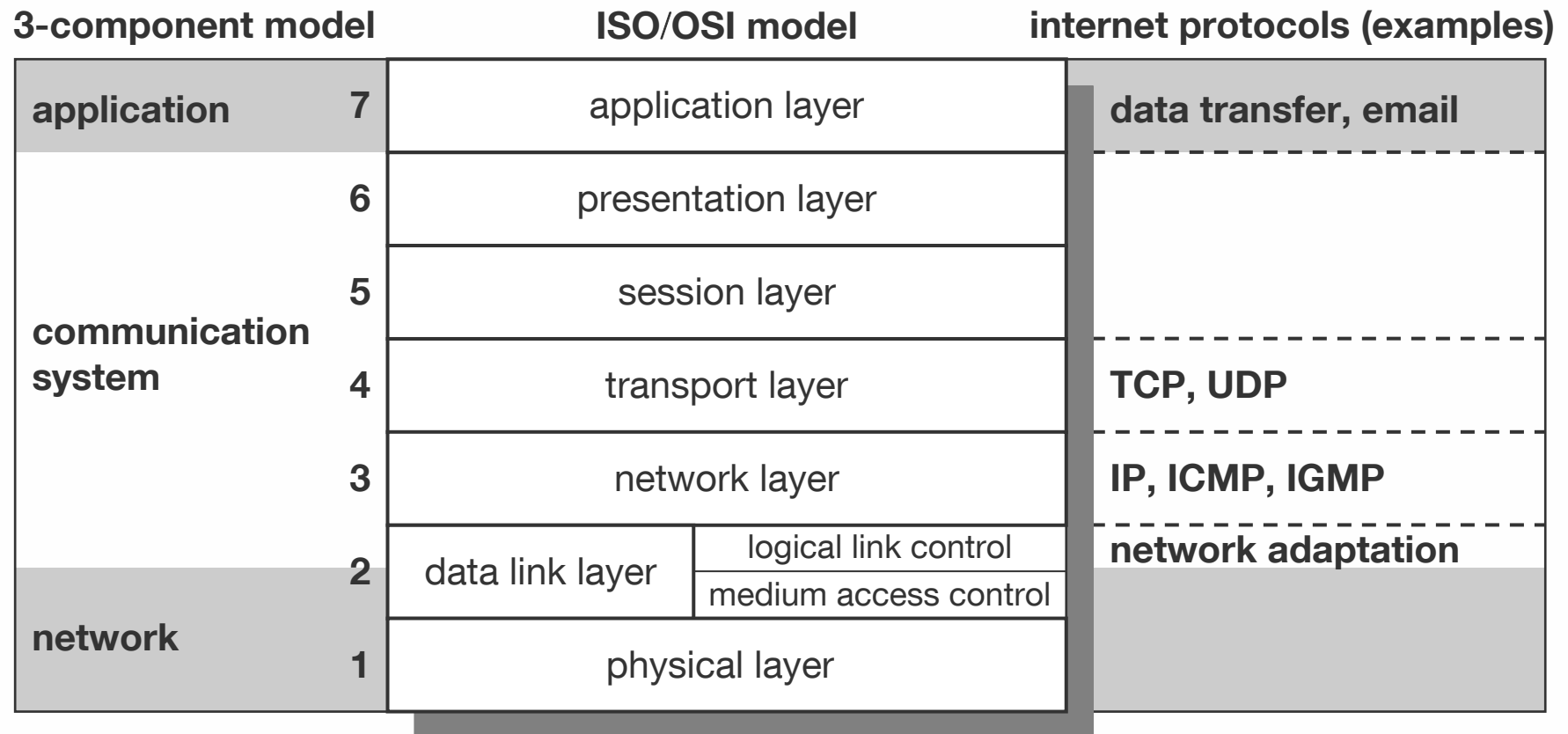
Examples

- in the past years, different (proprietary) high-performance networks have established on the market
- typically, these consist of
 - a static and / or dynamic network topology
 - sophisticated network interface cards (NIC)
- popular networks
 - Myrinet
 - InfiniBand
 - Scalable Coherent Interface (SCI)

2 High-Performance Networks

Examples

- reminder: protocols



2 High-Performance Networks

Examples

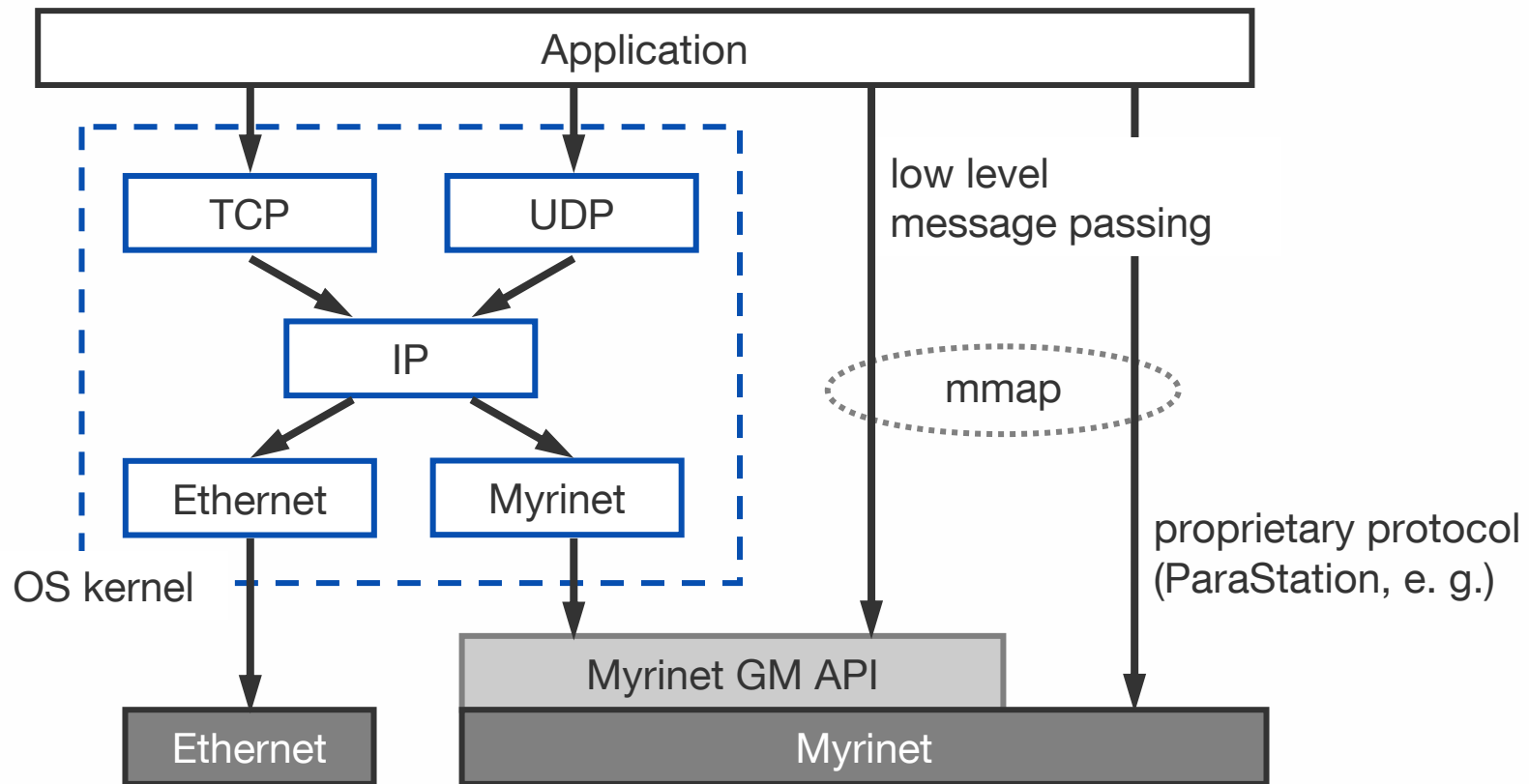
- Myrinet
 - developed in 1994 by Myricom for clusters
 - particularly efficient due to
 - usage of onboard (NIC) processors for protocol offload and low-latency, kernel-bypass operations
 - highly scalable, cut-through switching
 - latest product: Myri-10G
 - available for both copper and fiber cables
 - 10+10Gbps throughput (two-way for sending and receiving)
 - measured performance: 9.6Gbps one-way with 2.3 μ s latency
 - switching: rearrangeable non-blocking CLOS (128 nodes)
 - “spine” of CLOS network consists of eight 16 \times 16 crossbars
 - nodes are connected via line-cards with 8 \times 8 crossbar each
 - approx. costs 50,000€ for switch and 75,000€ for NICs



2 High-Performance Networks

Examples

- Myrinet (cont'd)
 - programming model



2 High-Performance Networks

Examples

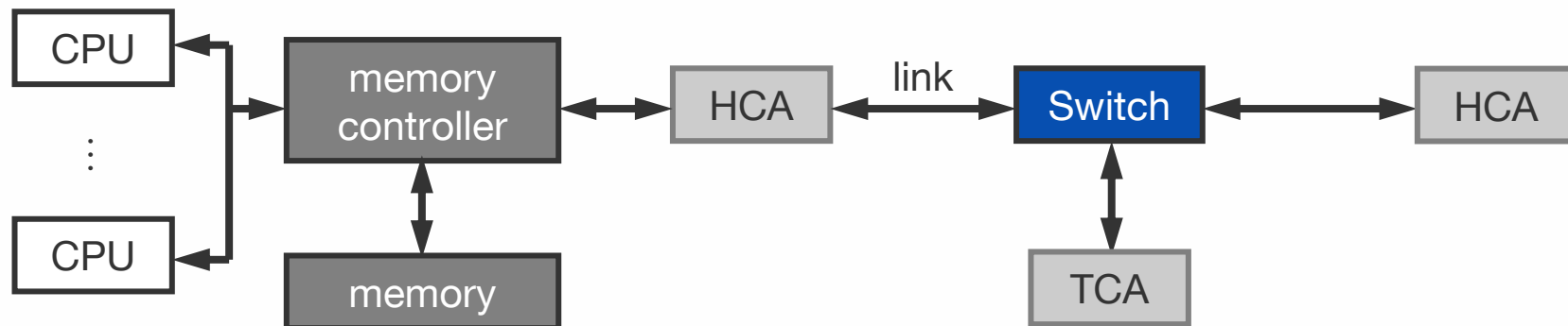
- **InfiniBand**
 - unification of two competing efforts in 1999
 - Future I/O initiative (Compaq, IBM, HP)
 - Next-Generation I/O initiative (Dell, Intel, SUN et al.)
 - idea: introduction of a future I/O standard as successor for PCI
 - overcome the bottleneck of limited I/O bandwidth
 - connection of hosts (via host channel adapters (HCA)) and devices (via target channel adapters (TCA)) to the I/O “fabric”
 - switched point-to-point bidirectional links
 - bonding of links for bandwidth improvements: 1× (2.5Gbps), 4× (10Gbps), 8× (20Gbps), and 12× (30Gbps)
 - available for both copper and fiber cables
 - nowadays only used for cluster connection



2 High-Performance Networks

Examples

- InfiniBand (cont'd)
 - particularly efficient (among others) due to
 - protocol offload and reduced CPU utilisation
 - Remote Direct Memory Access (RDMA), i. e. direct access (read and write) via HCA to local and remote memory without CPU usage and CPU interrupts



- switching: constant bisection bandwidth (up to 288 nodes)
- approx. costs 50,000€ for switch and 110,000€ for 128 NICs

2 High-Performance Networks

Examples

- **Scalable Coherent Interface**
 - originated as an offshoot from IEEE Futurebus+ project in 1988
 - became IEEE standard in 1992
 - SCI is a high performance interconnect technology that
 - connects up to 64,000 nodes (both hosts and devices)
 - supports remote memory access for read / write (NUMA)
 - uses packet switching point-to-point communication
 - SCI controller monitors I/O transactions (memory) to assure cache coherence of all attached nodes, i. e. all write accesses that invalidate cache entries of other SCI modules are detected
 - performance: up to 1GBps with latencies smaller than $2\mu\text{s}$
 - different topologies such as ring or torus possible

2 High-Performance Networks

Examples

- Scalable Coherent Interface (cont'd)
 - shared memory: SCI uses a 64-bit fixed addressing scheme
 - upper 16 bits specify node on which the addressed physical storage is located
 - lower 48 bits specify the local physical address within memory
 - hence, any physical memory location of the entire memory space can be mapped into a node's local memory

